REMARKS

Claims 1-6 and 10-24 are pending. Claims 1-6, 12, 13, and 19 have been amended, claims 7-9 have been canceled, and new claim 24 has been added to recite additional clarifying features of the embodiments disclosed in the specification.

Reconsideration of the application is respectfully requested for the following reasons.

In the Office Action, claims 1-23 were rejected under 35 USC § 103(a) based on a Hayashi-Chiussi combination. This rejection is traversed for the following reasons.

Claim 1 recites: (1) said at least one CPS packet is stored in one of the memories at a predetermined address indicated by a routing tag allocated to said at least one CPS packet by a corresponding one of the receiver circuits, and that (2) the two or more transmitter circuits search the memories to locate the multicast information and transmit the AAL2 packet based on the search results. These features are not taught or suggested by the cited references.

The Hayashi patent discloses a buffer 401 which stores a series of CPS packets included in a received AAL2 cell. The packets are then sent to an output port through an ATM switch 407. The Hayashi circuit, however, does not perform a multicasting operation. Accordingly, Hayashi fails to teach or suggest that "the two or more transmitter circuits search the memories to locate the multicast information and transmit the AAL2 packet based on the search results."

Furthermore, Hayashi discloses outputting CPS packets in buffer 401 to ATM switch 407 based on a switching tag. Unlike claim 1, this switching tag does not provide an indication of a predetermined address within buffer 401 for storing a CPS a packet. Rather, the switching tag of

Hayashi is used by switch 407 to route a CPS packet stored in buffer 401 as well as to perform internal processing functions in system 15. (See column 7, lines 7-20). The Chiussi patent fails to make up for these deficiencies.

The Chiussi patent discloses an ATM switch for performing a multicasting operation. The switch is disposed between a plurality of input ports and a plurality of output ports. In operation, a received ATM cell is stored in a memory (one of ABMs 0-5 in Fig. 1) associated with an input port. The switch then formulates a translation table 900 which is used to output and then route the stored ATM cell to one or more output ports in response to a multicast request.

However, unlike claim 1, the Chiussi patent does not disclose that the ATM cells are stored in the memories (ABM) "at a predetermined address indicated by a routing tag allocated to said at least one CPS packet by a corresponding one of the receiver circuits." Rather, Chiussi discloses that the addresses in the ABM memories are obtained from a linked list 1001 of free memory addresses (column 9, lines 27-31), i.e., whatever free memory addresses are available at the time. Thus, Chiussi does not teach or suggest storing ATM cell payloads in predetermined addresses indicated by a routing tag assigned to a CPS packet when it is separated from an AAL2 cell, as required by claim 1.

Incidentally, Chiussi mentions a connection tag 908 which is used to determine address information. However, as disclosed at column 5, line 64 - column 6, line 6, the connection tag is used to calculate an address in a Header Translation Lookup table, which stores information

indicating a new VPI/VCI to be assigned to an ATM cell to be multicast. This connection tag does not specify a predetermined memory address for storing a CPS packet received by one of the receiver circuits.

Furthermore, in Chiussi, the transmitter circuits (e.g., output port cards) do not perform the searching function recited in claim 1. That is, while the output cards are coupled to a switching circuit 130, the output cards do not search the ABM memories in the input port cards to locate multicast information and to transmit the AAL2 packet based on the search results. Rather, the output port cards merely receive stored ATM cells based on results of a look up function performed by switching circuit 130 based on information in translation table 900.

Thus, as described in detail in the specification (see, for example, page 13), at least one embodiment of the invention is considered to be superior to other systems (such as exemplified by Hayashi and Chiussi) based on the use of the routing tag and searching function performed by the transmitter circuits of claim 1. These features are not taught or suggested by Hayashi and Chiuss, whether taken alone or in combination. Accordingly, it is respectfully submitted that claim 1 and its dependent claims are allowable.

Claim 3 recites that a new virtual path virtual channel (VPVC) and the routing tag for at least one CPS packet are allocated based on a VPVC and a channel identifier (CID) in the received AAL2 packet. None of the cited references teach or suggest the routing of claim 1. Accordingly, it is respectfully submitted that these references do not teach or suggest allocating a new VPVC and the routing tag based on a VPVC and CID of a received AAL2 packet.

Claim 4 recites that "the at least one CPS packet and the new VPVC are stored at the predetermined address indicated by the routing tag." These features are not taught or suggested by the Hayashi and Chiussi patents, whether taken alone or in combination. For example, the Chiussi patent discloses generating a new virtual path for a received ATM cell. However, this new virtual path identifier is stored in the translation table 900, not with the CPS packet stored in a predetermined memory address designated by the routing tag. According, it is respectfully submitted that claim 4 is allowable, not only by virtue of its dependency from claim 1 but also based on the features separately recited therein.

Claim 5 recites that the "addresses for storing CPS packets in each of the memories are allocated to correspond to output ports coupled to the transmitter circuits." These features are not taught or suggested by the Hayashi and Chiussi patents, whether taken alone or in combination.

Claim 6 recites that each memory area allocated for storing CPS packets includes "a memory status field that stores information indicating whether a CPS packet is stored in said area, a copy port field that stores information indicating whether the stored CPS packet is to be multicast through two or more of the transmitter circuits, and a port area that stores the CPS packet with a new virtual path virtual channel (VPVC) generated for the stored packet based on at least one of a VPVC or a channel identifier (CID) of a received AAL2 packet." These features are not taught or suggested by the Hayashi and Chiussi patents, whether taken alone or in combination. For example, Chiussi discloses storing new virtual path information in a translation

table 900. However, this information is not stored with a CPS packet at a predetermined memory address indicated by a routing tag, along with the routing tag stored in another field included at that memory address.

New claim 24 recites that "each of the memories have predetermined address which correspond in number to a number of output ports coupled to the transmitter circuits, said predetermined addresses storing CPS packets received from corresponds ones of the receiver circuits." These features are not taught or suggested by the Hayashi and Chiussi patents, whether taken alone or in combination.

Claim 13 recites "storing the CPS packet and the new VPVC according to the routing information, the routing information indicating one or more predetermined storage areas in a memory allocated for storing the CPS packet" and of "extracting the CPS packet by searching the plurality of storage areas." These features are not taught or suggested by the Hayashi and Chiussi patents, whether taken alone or in combination. Accordingly, it is submitted that claim 13 and its dependent claims are allowable.

Claim 19 recites "storing the CPS packet according to a routing information, the routing information indicating a predetermined memory address allocated for storing the CPS packet." These features are not taught or suggested by the Hayashi and Chiussi patents, whether taken alone or in combination. Accordingly, it is submitted that claim 19 and its dependent claims are allowable.

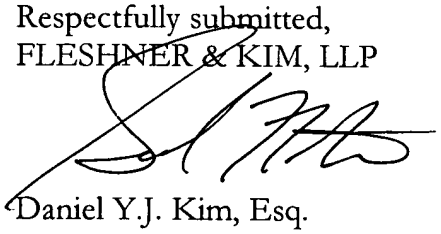
Claim 20 recites that "the routing information is generated based on a virtual path virtual channel (VPVC) and a channel identifier (CID) of the received AAL packet, and wherein a new VPVC is generated and stored based on the VPVC and the CID." The cited references do not teach or suggest the routing information of claim 19. Therefore, it logically follows that the features of claim 20 relating to the routing information are also missing from these references.

Claim 22 recites "periodically searching for a memory status field and a copy port field corresponding to each of a plurality of output ports." These features are not taught or suggested by Hayashi and Chiussi.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and allowance of the application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



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